WHAT IS CLAIMED IS:

1. A method of synchronizing a data stream between two distinct clock domains, said method comprising the steps of:

receiving said data stream at a rate of a first clock;

sequentially loading said data stream into a plurality of registers at said first clock rate;

utilizing a digital differential analyzer to generate a synchronization signal having a frequency proportional to a ratio of said first clock rate and a rate of a second clock; and

sequentially reading said plurality of registers at a rate corresponding to said frequency of said synchronization signal.

2. A method of synchronizing a data stream between two distinct clock domains according to claim 1, wherein said sequential loading of said data stream comprises:

loading an x^{th} word of said data stream into a y^{th} register of said plurality of registers during a first clock cycle of said first clock; and

loading an $x^{th}+1$ word of said data stream into a $y^{th}+1$ register of said plurality of registers during a second clock cycle of said first clock.

3. A method of synchronizing a data stream between two distinct clock domains according to claim 1, wherein said sequential loading of said data stream comprises:

wherein for said plurality of registers comprising y registers, each register is reloaded with a new word of said data stream every $y^{th}+1$ cycles of said first clock.

4. A method of synchronizing a data stream between two distinct clock domains according to claim 1, wherein said synchronization signal comprises M pulses every N cycles, said M pulses being distributed substantially evenly throughout the N cycles.

5. An apparatus for synchronizing a data stream between two distinct clock domains, said apparatus comprising:

an input means for receiving said data stream at a rate of a first clock;

a means for sequentially loading said data stream into a plurality of registers at said first clock rate;

a digital differential analyzer operative for generating a synchronization signal having a frequency proportional to a ratio of said first clock rate and a rate of a second clock; and

a means for sequentially reading said plurality of registers at a rate corresponding to said frequency of said synchronization signal.

6. The apparatus for synchronizing a data stream between two distinct clock domains according to claim 5, wherein the means for sequentially loading said data stream comprises a rotate register having a predetermined length corresponding to the total number of registers forming said plurality of

registers, said rotate register having an output coupled to each of said plurality of registers, said rotate register operative for sequentially enabling each of said plurality of registers to store a word of said data stream.

7. The apparatus for synchronizing a data stream between two distinct clock domains according to claim 5, wherein the means for sequentially reading said plurality of registers comprises:

a multiplexer operative for selecting one of said plurality of registers to be read; and

a rotate register coupled to said multiplexer and operative for controlling said multiplexer such that said multiplexer sequentially reads said plurality of registers at a rate corresponding to said synchronization signal.

8. The apparatus for synchronizing a data stream between two distinct clock domains according to claim 5, wherein said synchronization signal comprises M pulses every N cycles, said M pulses being distributed substantially evenly throughout the N cycles.